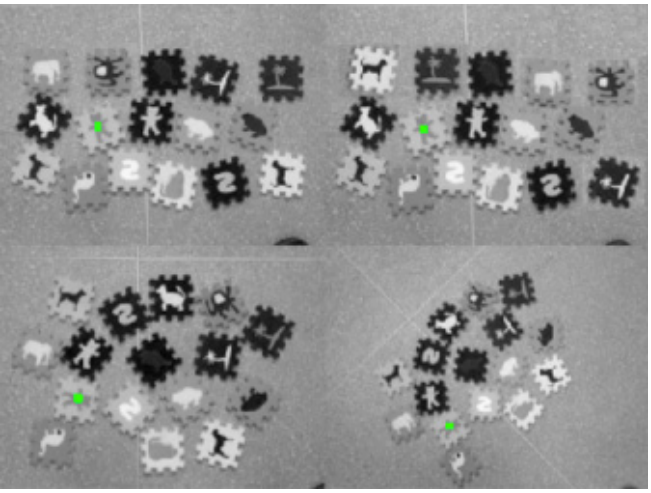

XFV

eXtremely Fast Vision

Project Summary

The goal of this project is to detect a given pattern in an image by applying an adequate algorithm. The problem is complex because the pattern we look for can be : *shifted*, *rotated* or *scaled*.

To alleviate these 3 constraints and to be compatible with real time constraints imposed by the industrial environment, the brute force algorithm based on a full correlation can not be considered.

The originality of this project is based on the use of a projection algorithm which converts a 2D problem into two 1D problem, radial and circular, reducing greatly the complexity by keeping the performance at a high level.

In this project, the selected CIRATEFI projection algorithm has been simulated and implemented on :

- A PC in Matlab
- A PC in C by using the OpenCV library
- An FPGA

The obtained results are good in term of robustness to noise and processing speed. Two life demos, one with a PC and the other with a dedicated FPGA embedded system have been presented to the ISYS committee on the presentation day. These demos were fully real-time which a great performance considering the complexity of the problem.

Valorisation

This project was originally initiated by a discussion with the Bobst SA company. It has been already presented with success to the ISYS meeting and will be shortly to the Bobst SA R&D managers. The results of this project will be discussed in several bachelor and master level courses as an example of complexity reduction by use of a projection algorithm.

An interesting by-product of this project lies in the methodological approach which has been used. This was based on :

1. A complete simulation of the CIRATEFI on Matlab. In this phase, the robustness of the method to noise was determined and quantized.
2. The algorithm was then re-written in C by using the state of the art OpenCV library and the results compared to the ones provided in the first phase.
3. Finally, an FPGA design was done and the results compared to the first phase. It has to be noticed that the FPGA results were not as good as the ones provided in the simulation phase. After inquiry it comes out that the use, at a given stage of the design, of numbers with limited precision was the cause of the problem.

Contact / Michel Kocher (michel.kocher@heig-vd.ch)

This project has been carried out by the IAI (HEIG-VD) in collaboration with REDS (HEIG-VD) and HES-SO Valais