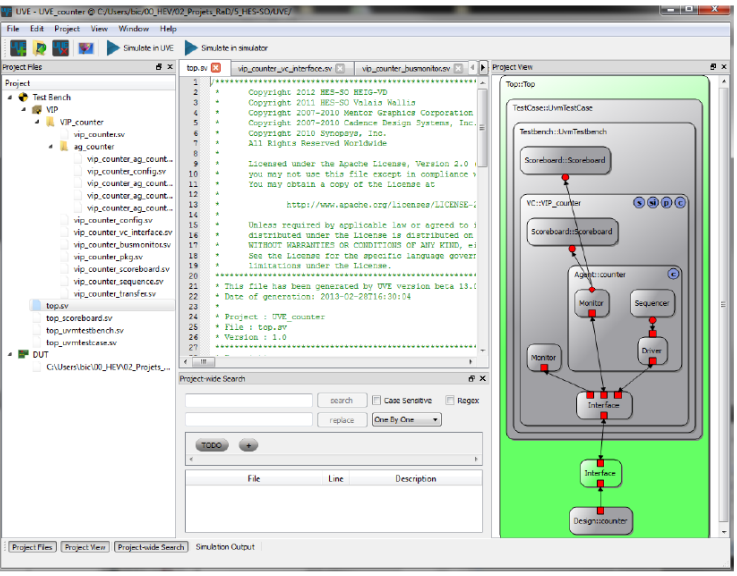

UVE, UNIFIED VERIFICATION ENVIRONMENT

A tool to automatically generate a testbench in SystemVerilog

Project Summary

The increasing complexity of digital systems disrupts the development process in the sense that the verification of these designs is becoming longer. To reduce the verification time, manufacturers of industrial EDA tools offer more sophisticated ways, particularly through the use of verification languages like SystemVerilog. Some verification IPs (Intellectual Property) are also beginning to appear, to accelerate the verification process.

However, learning these new tools and new methodologies requires a significant investment from the industry. Their complex implementation and cost are often an obstacle to their introduction. It therefore becomes necessary to offer manufacturers the means to support them in this transition and increase the return on investment of implementing such tools and methodologies.

In this context, the aim of the UVE project is to create a software tool capable of automatically generate a verification testbench written in SystemVerilog and integrating the UVM methodology. It allows to rapidly being in possession of a verification environment capable of performing simulation on a DUV (design under verification). UVE includes a graphical user interface, a code generator, compilation scripts and a library of verification IPs (VIP). One of the main innovations resides in the fact that this tool proposes to the user a todo list for testbench finalization.

Moreover, the graphical interface lets the user observe the testbench structure that is generated. Files can be accessed easily by double clicking on the graphical view. Simulation can be launched directly from the tool.

UVE is now an operational framework that can be used as is. Some improvements could take the form of adding new VIPs in the library.

Valorisation

UVE is an open source software. A website (http://www.systemverilog.ch) presents the results of the project, and supplies the source code in order to allow other developers and teams to participate to this project by improving it. An article will be submitted to Alliance for publication. Moreover, the competences acquired, especially in SystemVerilog, already served in other projects, as well as in master courses.

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