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SSAC

Computer Acceleration based on FPGA and USB3 SuperSpeed link

Project Summary

Hardware accelerators on the market today are often cards plugged into desktops. This project comes from a new vision of hardware acceleration in the PC world: a hardware accelerator module including a programmable component (FPGA) is connected to a PC through a SuperSpeed USB 3.0 Link.

The main objectives of this project were to manage the USB 3.0 connection, to optimize data transfers between the PC and the device and to provide a framework including generic software and hardware blocks (VHDL interface code, drivers, API). Thanks to the reuse of generic parts and the automatic generation of specific parts, this framework allows easy developing of applications with hardware acceleration.

A demonstrator - based on a FPGA /USB3.0 COTS board connected to a laptop – has been developed. An application on laptop runs an image processing algorithm on a video stream. Due to the heavy computation load of the image processing algorithm, the processor is not able to sustain the frame rate. The algorithm is implemented on the hardware accelerator. The images are sent to the accelerator, processed and then sent back, thus demonstrating that the image processing with hardware acceleration is done in real time without any frame rate slow-down.

Valorisation

Hardware acceleration is a very efficient solution when an application is running too slowly on a PC, rather than to increase CPU computational power by moving application to high performance server or even cluster of servers. Our USB3 approach is especially attractive when the application to accelerate is running on a laptop. An USB3 accelerator module is small, light, low power and easy to install.

Applications of hardware acceleration are numerous. We can mention some of them in different domains (biology, medical, engineering, mathematical, financial…): data market, trading, genomic, statistics, simulation, modeling, image processing.

Our approach should interest the developers of CPU power consuming code, the users of applications needing long computation time (in research labs as example), or even the manufacturers of FPGA boards.

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This project has been carried out by HEIG-VD (REDS Institute)

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