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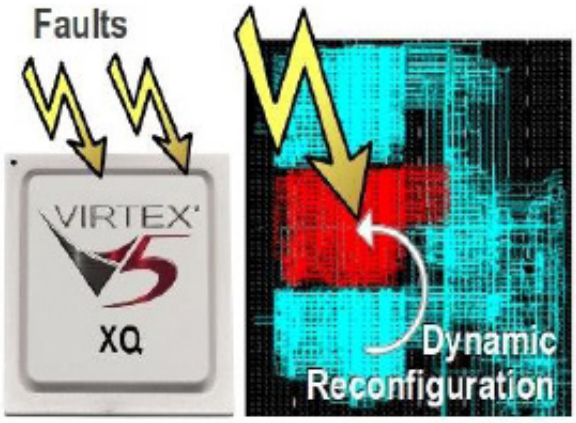

REDTOP

Fault Tolerance through FPGA Dynamic Reconfiguration

Project Summary

Current commercial FPGA from Xilinx can be partially reconfigured in a dynamic way. Partial dynamic reconfiguration offers the possibility of retargeting the logical systems implemented in the FPGA in order to reuse the available configurable logic for supporting different hardware systems. This feature allows reducing hardware resources requirements, reducing cost and power consumption, while enhancing the flexibility and capabilities of the system in the form of a virtually infinite number of possible partial configurations to implement on a device.

The main goal of this project is to contribute to fill the gab between the high potential offered by the technology and its use on industrial applications. It is materialized with the setup of a dynamically and partially reconfigurable platform composed of a set of redundant modules on a state-of-the-art commercial FPGA. We developed a set of techniques and tools that mitigate SEU faults on Virtex-5 FPGAs through the use of dynamic partial reconfiguration.

This fault-tolerance technique provides fault mitigation by verifying architectural integrity. The key idea is to reconfigure the damaged part of the configuration bitstream in order to repair the bitstream and, thus, the overlying architecture. The first step is to detect a fault, the system to be enhanced with fault mitigation is triplicated and its configuration bitsream is continuously read and compared among the triplicated modules. When a fault is detected only the damaged part of the system is reconfigured, while the others modules continue their task execution.

To this end, we proposed a design flow and a set of tools that allow us to manipulate the bitstream generation. As case study, we present an application using an AES encryption coprocessor, a fault detection system constantly verifying system integrity and repairing faults, and an independent program injecting faults to validate the sysem.

Valorisation

The valorisation of this project is mainly represented by a demonstrator, and by the visibility obtained in the specific domain of dynamically reconfigurable digital systems. Three aspects that can assess this visibility: the presentation and publication of our work in the international conference Reconfig 2012, the invitation to present this project to industries and international universities, and the invitation to participate on two European project consortiums.

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This project has been carried out by HEIG-VD (REDS Institute)

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