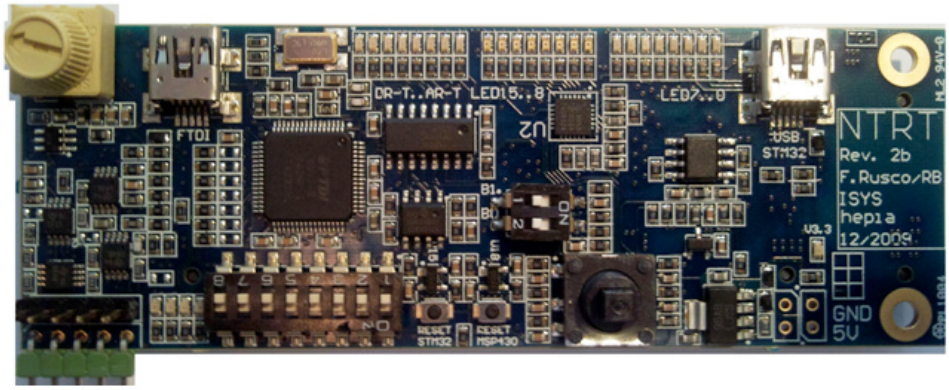

NTRT

Power-aware Real-Time Kernel with Soft Deadlines

Project Summary

Many embedded applications are based upon hard real-time schedulers where each task deadline must be met and designed under worst-case situations where tasks have worst-case executing times, minimum arrival intervals and minimum deadlines. Such designs usually result into an overly sized system having poor resource utilization. On the other hand, by not having to meet every deadline, the system becomes simpler and more cost-effective while taking greater advantage of the available resources. In NTRT, tasks are specified by an (*m*,*k*)-constraint where *m* is the least number of deadlines that should be met out of *k* consecutive task invocations. The remaining *k*-*m* tasks are dispatched only if the task can meet its deadline. Tolerating deadline misses in this way, given that they occur in a clear predictable and bounded manner, has the following advantages: alleviating the consequences of pessimism in the system parameters, providing a mechanism that allows a controlled and fair degradation of quality of service, allowing transient overload without jeopardizing the scheduling of the tasks, and all task executions contribute to add value to the system since none are done purposelessly.

The second innovative aspect of NTRT is its dynamic power management scheme that takes advantage of the processor's deep-sleep modes and which can save more than a 1000-fold amount of energy compared to regular sleep modes. The scheme becomes effective for a breakeven of approximately 4 ms on a ST Microelectronic's 32-bit STM32 Cortex-M3 microcontroller. The NTRT scheduler implements an aggressive algorithm that maximizes the length of the idle intervals by delaying the wake-up of the processor while guaranteeing that the specified task deadlines requirements are still met.

To validate the concepts, a specific design has been realized based on 2 processors: a STM32 Cortex-M3 microcontroller that is power optimized by the NTRT kernel, and a MSP430, a 16-bit microcontroller from TI, with very low-power consumption (~1 µA). This second processor manages the wake-up of the first one.

Valorisation

NTRT is an innovative kernel that may easily be ported on a number of 16- or 32- microcontrollers having soft real-time requirements. As current IC technology continues to scale-down, leakage power consumption is becoming a significant part of overall power consumption. To this end, NTRT clearly demonstrates the feasibility of merging scattered idle intervals to reduce the shut-down and wake-up overhead and greatly improves energy performance.

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