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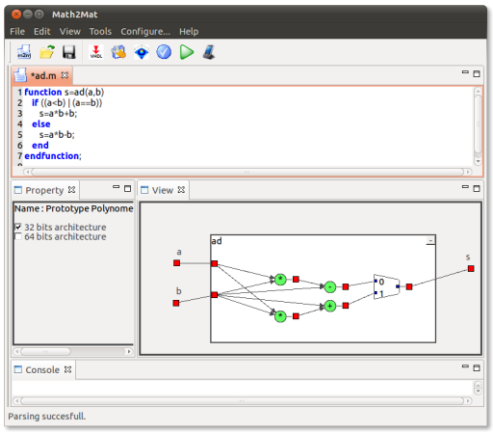

MATH2MAT

A tool to automatically translate Matlab code into a HDL description

Project Summary

Common processors can obviously perform mathematical calculation, but Field Programmable Gate Arrays (FPGA) allow to take advantage of the inherent parallelism of hardware in order to speed up such processing. However, developing efficient FPGA solutions is not as straightforward as their purely software counterpart.

In this context, the aim of the Math2mat project was to create a software tool capable of automatically generate a synthesizable HDL description of a mathematical function written in Matlab/Octave. It allows to rapidly being in possession of a VHDL entity capable of performing efficient calculation. One of the main innovations resides in the fact that the operations are executed on floating point numbers of 32 or 64-bit. Basic operators (+,-,*,/,square root) have been developed, both in a combinatorial and a pipeline way, and are now freely available.

These operators are then combined in order to generate a hardware structure performing a function such as the one illustrated on the picture. Control structures such as *if/then/else* as well as *for loop* can be synthesized, and the structure is optimized in order to offer up to one operation per clock cycle. The *for loop* mechanism is one of the main achievements of the project. It accepts up to *n* input operations for a pipelined body loop of depth *n*, and embeds a reorder buffer that allows pipelining calculation in the form "*for I in 0:a*", where *a* may vary. The system is based on a self-regulating auto-delay mechanism that allows to freeze the calculation from the module getting the output of the computation. Moreover, the graphical interface lets the user observe the structure that would be generated, and to select the kind of computational block has to be used for any of the operations. This graphical interface is automatically updated during code typing, and allows to rapidly have an idea of the hardware structure derived from any specific Matlab/Octave code.

A verification testbench is also automatically generated, and a simulation can be launched by the application, in order the user to fully trust the VHDL he gets. The testbench is based on SystemVerilog, and could allow to develop new implementations of operators or new functions (sin, cos, …) and to test rapidly validate them. Math2mat is now an operational framework that can be used as is. Some improvements could take the form of adding new operations (sin, cos, …), adding new data types (fixed point numbers, decimal floating point).

Valorisation

Math2mat is an open source software. A website (http://www.math2mat.ch) presents the results of the project, and supplies the source code, in order to allow other developers and teams to participate to this project by improving it. An article will be submitted to Alliance for publication, and a seminar will be organized in order to disseminate the results. Moreover, the competences acquired, especially in SystemVerilog, already served in other projects, as well as in master courses.

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This project has been carried out by HEIG-VD, hepia, EIA-FR, HES-SO//VS, HE-Arc

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