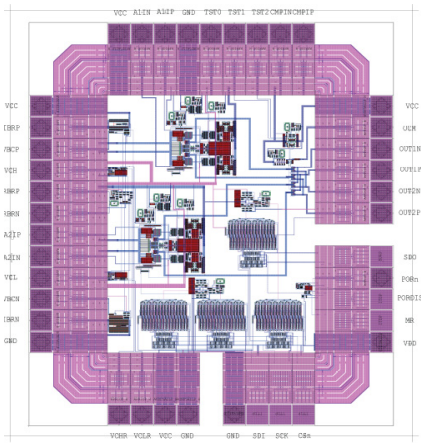

FEITUS

Integrated front-end for ultrasound transducer

Description

Applications using ultrasound transducers for emission of strong pulses and reception of their weak echoes have to deal with a very high dynamic range. At the beginning of the receiver chain, the low noise amplifier (LNA) is prone to overload and thus recovery problems.

The goal of this project was to design a low noise differential amplifier architecture with a very fast and clean overload recovery behavior. Transistor saturation and self-heating effects have been carefully studied and taken into account. This design has been integrated on a 0.35 µm BiCMOS SiGe technology featuring npn bipolar transistors with a f_T of 70 GHz.

For clamping of input voltages higher than about 1.0V, an external Schottky diode bridge with on chip control and active biasing has also been designed and integrated. This bloc is completely independent of the other blocs of the chip and could lead to the development of a standard IC.

The main simulation results are: bandwidth ≈ 10 GHz, overload recovery time <10 ns, input referred noise < 2.0 $nV/Hz^{0.5}$. The 2.973 mm^2 chip has been mounted into a 7 x 7 mm high frequency package and tested. Simulations and measurements have shown good agreements for most of the functionality. However, more accurate high frequency characterisation would still be needed to fully validate the concepts.

Knowledge gained by this project helped to address also a time of flight mass spectrometer (TOF-MS) signal conditioning project where this kind of problems is also encountered.

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